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A Four-Terminal TiO_{2-x} Memristor Architecture Enabling Multidimensional Associative Learning

Ryohei Yamamoto¹ | Yusuke Hayashi^{1,2} | Zhuo Diao¹  | Tetsuya Tohei¹  | Akira Sakai^{1,3} 

¹Graduate School of Engineering Science, The University of Osaka, Toyonaka, Osaka, Japan | ²National Institute for Materials Science (NIMS), 1-2-1 Sengen, Tsukuba, Ibaraki, Japan | ³Spintronics Research Network Division, Institute for Open and Transdisciplinary Research Initiatives, The University of Osaka, Suita, Osaka, Japan

Correspondence: Tetsuya Tohei (tohei@ee.es.osaka-u.ac.jp) | Akira Sakai (sakai@ee.es.osaka-u.ac.jp)

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ABSTRACT

Associative learning, a key higher-order function of biological synapses, remains challenging to implement in hardware due to limitations in existing memristor architectures. Here we develop a four-terminal TiO_{2-x} memristor enabling two-dimensional control of oxygen vacancy distributions, exhibiting stable non-filamentary resistive switching accompanied by visible electrocoloring with applied voltages. Using a single four-terminal device, we demonstrate bidirectional Pavlovian conditioning encompassing both learning and forgetting processes. Furthermore, by arranging multiple memristors based on this architecture, multidimensional associative learning of two-dimensional image data is realized without involving any external circuits or computing units. These findings indicate that the proposed memristor architecture functions as a self-contained physical learning element capable of acquiring and updating associations between stimuli. This work thus provides a conceptual framework for neuromorphic hardware that implements higher-order associative functions, advancing beyond conventional software-based artificial neural networks.

1 | Introduction

Biological synapses are the fundamental units of information transmission in brains, where synaptic strength is dynamically modulated by the propagation of action potentials, enabling processes such as learning and forgetting [1–3]. In contrast, a memristor is a passive device typically composed of a two-terminal structure, in which the distribution of dopants within the device is modulated by an applied voltage, particularly in non-filamentary types, resulting in a change in resistance (or conductance) [4, 5]. By correlating these conductance changes with synaptic plasticity, memristors have attracted significant attention as artificial synapses for hardware-based neural networks [6–15].

In parallel with advances in software-based artificial neural networks (ANNs), there has been rapid progress toward implementing such learning functions in hardware using artificial

synaptic memristors. ANNs proposed so far rely on deterministic computational structures that generate outputs solely from specified inputs, which entail functional limitations. By contrast, biological synapses determine their outputs through higher-order mechanisms that involve not only principal neurons but also modulators such as interneurons, neuromodulators, and glial cells. One of the most representative forms of such higher-order functionality is associative learning, a process through which adaptive responses are acquired based on the prediction of reward or punishment outcomes. Realizing neuromorphic hardware with such associative learning functionality is therefore essential for advancing the sophistication of artificial intelligence (AI) systems.

While many memristor devices have been used to implement supervised and unsupervised learning in hardware, there is a growing interest in demonstrating associative learning directly on electronic devices. We have previously demonstrated

[Correction added on 9 September 2026, after first online publication: The second affiliation has been newly added.]

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non-filamentary resistive switching in devices based on reduced titanium oxide (TiO_{2-x}) and gallium oxide (GaO_x) [16–24]. A distinctive feature of our approach lies in adopting a four-terminal memristor architecture. This architecture allows two-dimensional (2D) distribution modulation of oxygen-vacancies as dopants, rather than one-dimensional connection/rupture of conductive filaments, and brings deterministic resistive change behaviors. This enables advanced synaptic functionalities, such as precise synaptic weight control (high-resolution analog resistive change) [24], tunable heterosynaptic plasticity [25, 26], and Pavlovian-conditioning-based associative learning [20]. However, most demonstrations to date have been made at the binary level—“learning occurs or not,” corresponding to a single-bit signal—and thus fall short of the complex associative capabilities of biological systems. Given that modern AI applications require real-time processing of multidimensional and multilevel signals such as speech and images, it is imperative to move beyond one-bit conditioning and pioneer a neuromorphic hardware architecture that achieves extended associative learning over multibit signals, an area where studies remain limited [27, 28].

In this work, we fabricate and electrically characterize four-terminal planar TiO_{2-x} memristors to extend Pavlovian-conditioning-based associative learning to higher dimensions. To enable multidimensional associative learning, we investigate driving conditions that allow the device to exhibit both learning and forgetting, thereby demonstrating bidirectional Pavlovian conditioning within a single device. Furthermore, by operating multiple devices simultaneously, we achieve associative learning of two-dimensional 25-bit image data using only memristors without the need for any external circuits.

2 | Experimental Methods

2.1 | Fabrication of the Four-Terminal Memristor Architecture

A single-crystal rutile TiO_2 substrate was ultrasonically cleaned sequentially in acetone and isopropyl alcohol for 5 min each. A 40-nm thick TiO_{2-x} film was then grown on the insulating TiO_2 substrate using the pulsed laser deposition (PLD) technique. The deposition was carried out under the following conditions: a laser fluence of 70 mJ per pulse, an oxygen partial pressure of 1×10^{-4} Pa, and a substrate temperature of 500 °C. The deposited film exhibited a resistivity of $6.26 \times 10^{-3} \Omega\text{cm}$, confirming its moderately reduced conductive nature. The epitaxial growth of the TiO_{2-x} layer on the substrate was verified in situ using reflection high-energy electron diffraction (RHEED), as shown in Figure S1. The fabrication process of the four-terminal planar memristor architecture was designed with future device integration in mind (Figure 1a). First, for the bottom electrode layer, polymethyl glutarimide (PMGI) was spin-coated onto the TiO_{2-x} -deposited substrate and baked at 190 °C. A second resist layer of OFPR was subsequently applied and baked at 120 °C. Patterning of the electrode geometry was performed using a maskless lithography system (DDB-701-MS, NEOARK), followed by development in a tetramethylammonium hydroxide (TMAH) solution. A Pt layer was deposited via direct current (DC) sputtering, and the lift-off process was carried out in dimethylacetamide to define the bottom electrode. Subsequently, a 100-nm thick SiO_2 film

was deposited by radio-frequency (RF) sputtering to serve as the insulating layer. Contact vias connecting the bottom and top electrodes were then opened in the SiO_2 layer by maskless photolithography and chemical etching using a dilute hydrofluoric acid (HF) solution. Finally, Ti/Pt bilayer top electrodes were deposited onto the contact regions by DC sputtering to complete the four-terminal device structure. An optical micrograph of the fabricated miniaturized memristor is presented in Figure 1b, showing a terminal spacing (T1–T3) of 14 μm . This configuration allows for in-plane two-dimensional control of oxygen-vacancy migration, a key feature of the proposed memristor architecture.

2.2 | Electrical Characterization

All electrical measurements were carried out using a semiconductor parameter analyzer (Keysight B1500A) connected to a micromanipulator probe station inside a vacuum chamber at a base pressure below 10^{-3} Pa. The electrical terminals (T1–T4) of the four-terminal architecture were individually contacted using tungsten probe tips to ensure low-resistance connections. For each measurement, the conductance of the device was calculated from the current measured between terminals T1 and T3 under an applied read voltage of 1 V. This configuration was used to monitor the conductance variation during consecutive voltage applications to the other terminals (T2 and T4). All measurements were automated and computer-controlled to ensure temporal precision and repeatability across sequential conditioning experiments.

3 | Results and Discussion

3.1 | Fundamental Characteristics

Figure 2a shows the structure and definition of four terminals in the TiO_{2-x} memristor architecture. The planar configuration with four electrode terminals T1 to T4 enables control of the two-dimensional oxygen vacancy distribution. The fabricated devices exhibit stable non-filamentary resistive switching behavior, confirming the functional robustness of the proposed architecture. We first examined the basic characteristics of the four-terminal planar TiO_{2-x} memristor. Conductance between T1 and T3 (G_{1-3}) was read by applying a voltage V_1 to T1 while grounding T3. A write voltage $V_{2,4}$ was then applied simultaneously to T2 and T4 for 100 s with T1 and T3 grounded. This operation was repeated by ramping the voltage $V_{2,4}$ up and down over the range between the maximum voltage V_M and the minimum voltages V_m in 1 V steps. As shown in Figure 2b,c, when positive voltages were applied to T2 and T4, G_{1-3} entered a high-conductance state (HCS), while G_{2-4} entered a low-conductance state (LCS); under negative voltages, the pair inverted. The transition between the HCS and LCS exhibits a threshold-like change at an absolute applied voltage of approximately 5 V. This reversible switching between approximately 2.5 mS and 0.5 mS is attributed to the redistribution of oxygen vacancies. Figure 2d shows electrocoloring in the device as observed by optical microscopy. The appearance of dark-blue contrast near T1–T3 or near T2–T4 is consistent with the migration and accumulation of positively charged oxygen vacancy donors toward the grounded side or the biased side, thereby explaining the observed changes in G_{1-3} .

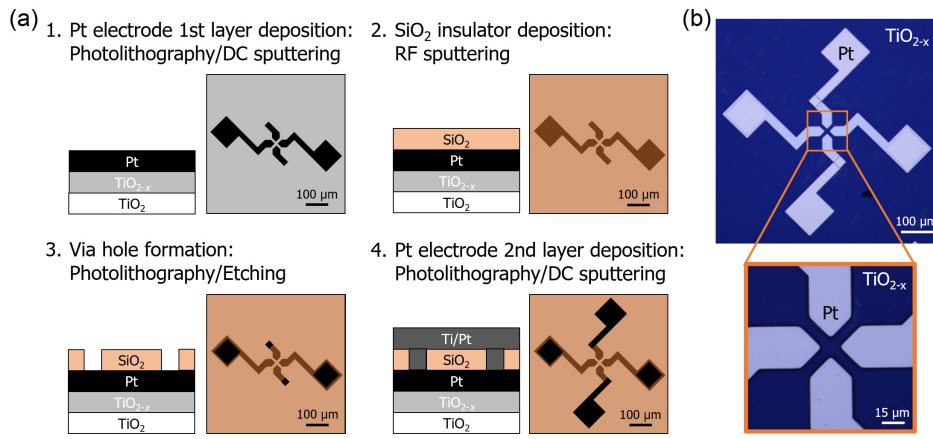


FIGURE 1 | (a) Device fabrication flow. (b) Plan-view optical micrograph of a fabricated four-terminal planar TiO_{2-x} memristor.

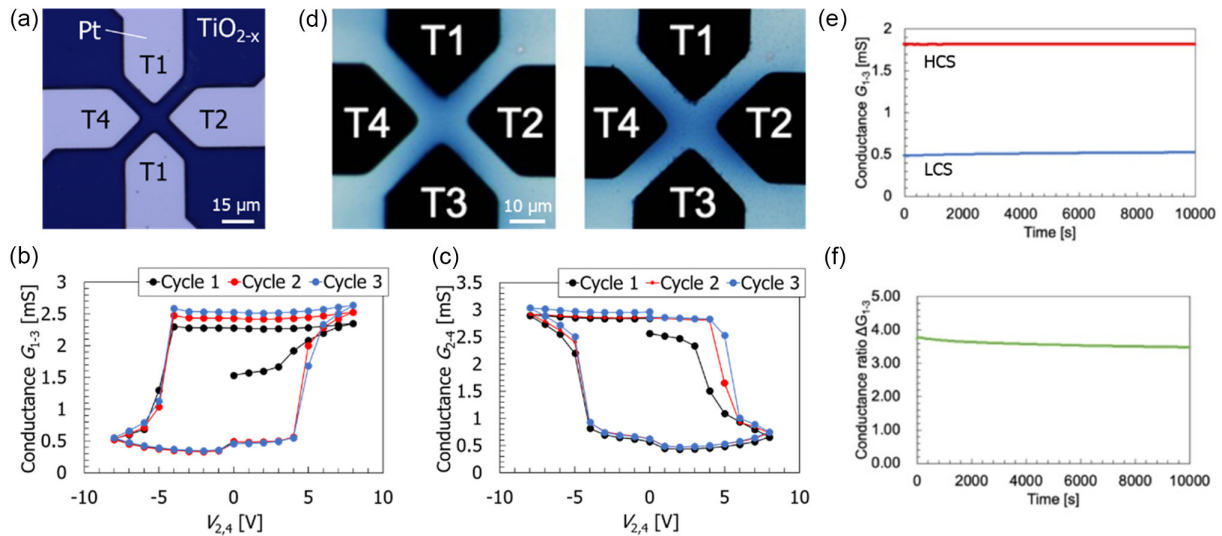


FIGURE 2 | (a) Optical micrograph of a four-terminal planar memristor fabricated on a TiO_{2-x} epitaxial thin film. (b) Variation of G_{1-3} and (c) G_{2-4} with $V_{2,4}$ with $V_M = +8\text{ V}$ and $V_m = -8\text{ V}$, where the cycle was repeated three times. (d) Optical micrographs showing internal structure of device just after application of $V_{2,4} = +8\text{ V}$ (left) and $V_{2,4} = -8\text{ V}$ (right) in cycle 3. (e) Retention characteristics of LCS and HCS in the four-terminal planar TiO_{2-x} memristor. (f) Time evolution of the On/Off ratio between LCS and HCS shown in (e).

for HCS or LCS, respectively. We can trace the oxygen vacancy redistribution inside the device by observing changes in the brightness within the resistive layer. The quantitative relationship between the observed optical contrast and the oxygen vacancy concentration is discussed in the Supporting Information.

Figure 2b,c show that the resistive change between HCS and LCS in the loop characteristics is stable over three cycles. Our previous study on the same type of devices have proven a good reproducibility of the loop characteristics among different devices and endurance over 30 cycles of potentiation/depression (or learning/forgetting) processes by pulse voltages, which is relied on deterministic resistive change brought by 2D redistribution of oxygen vacancy dopants [24].

The retention characteristics were evaluated by setting the device into LCS by negative $V_{2,4}$ sweeps and into HCS by positive $V_{2,4}$ sweeps, followed by repeated readout at fixed intervals up to 10^4 s . As shown in Figure 2e,f, both states remained stable throughout the

observation window, and the on/off ratio was maintained over time, respectively, indicating that the resistance states are highly time-stable—an essential requirement for preserving synaptic weights in neuromorphic applications.

3.2 | Bidirectional Associative Learning in Single Four-Terminal Memristor

Next, we demonstrate a realization of bidirectional associative learning employing a single four-terminal TiO_{2-x} memristor. To implement the conditioning process due to multiple associative inputs on a four-terminal memristor, the conductance states between each terminal are configured following our previous experimental procedure [20]. Here, we assign input voltage on T1 (V_1) as conditioned stimulus and voltage on T4 (V_4) as unconditioned stimulus. Conditioning states are represented by the conductance between T1 and T3 (G_{1-3}). In the classic example of Pavlovian conditioning, conditioned

stimulus V_1 corresponds to the “bell” and unconditioned stimulus V_4 corresponds to the “food”. Here, the oxygen vacancy distribution is initialized such that G_{1-3} is in LCS, while G_{4-3} is in HCS, corresponding to no response to the bell and the natural response to food. Then, voltage pulses (100 ms width) are applied to T1 (V_1) and T4 (V_4)—serving as the conditioned and unconditioned stimulus, respectively, while G_{1-3} monitors the conditioned response (Figure 3). Specifically, a single unconditioned pulse (V_4) was simultaneously applied once for every ten consecutive conditioned pulses (V_1). This process corresponds to forward conditioning (learning). Crucially, to achieve the multidimensional and multibit associative learning discussed later, it is also essential to realize reverse conditioning (forgetting). The process corresponds to driving G_{1-3} , once conditioned into the HCS, back to the LCS, which is accomplished by inverting the polarities of V_1 and V_4 . Figure 3 shows the voltage application protocol of V_1 and V_4 and measurement results of G_{1-3} . For the first LCS-to-HCS conditioning, a conditioned voltage of $V_1 = -4$ V and an unconditioned voltage of $V_4 = +4$ V were applied for the initial 50 cycles, followed by $V_1 = -5$ V and $V_4 = +5$ V for the subsequent 50 cycles. The results show that conditioning was not induced under an absolute voltage of 4 V (during the first 50 cycles). However, when the voltage amplitudes were increased to 5 V, the conductance exceeded the threshold value (1.0 mS) upon the third V_4 application (at pulse #80), indicating successful conditioning. Subsequently, HCS-to-LCS conditioning was performed by reversing the voltage polarities ($V_1 = +5$ V and $V_4 = -5$ V). In this case, the conductance G_{1-3} fell below the threshold value immediately after the V_4 application (pulse #110), confirming the realization of reverse conditioning or unlearning/forgetting. In the second trial, absolute voltages of 4 V were again employed for both LCS-to-HCS and HCS-to-LCS conditioning processes. The LCS-to-HCS switching was completed at the first conditioning (pulse #160), suggesting that the device response was facilitated by prior learning history. These results indicate that a bidirectional associative learning loop—learning and forgetting—can be achieved in a single memristor, thereby establishing the device-intrinsic programmability of the associative learning process. Concerning the power consumption during the conditioning process, we estimated it by using the following formula: $W_{\text{Pavlovian}} = G_{1-3} \times V_{\text{bell}}^2$. From G_{1-3} values in Figure 3, we estimated that power consumption at the Pavlovian conditioning before and after the conditioning was 17.5 mW (29.6 mW) and 35.0 mW (105.6 mW), respectively (those values for our

previous device with electrode distance of 70 μm [20] shown in parentheses). These values are not as small as those of the latest synaptic devices, but we achieved a 40% and 67% reduction in power consumption by employing an 80% reduction in device size using photolithography (14 vs. 70 μm electrode distances). We can expect a substantial reduction in power consumption with further reduction of the device size.

3.3 | Dimensional Extension of Associative Learning

The above investigation deals with a single memristor that performs associative learning based on one-bit zero-dimensional state transitions between the LCS (unlearned) and HCS (learned). Next, we examine the extension of associative learning functionality using two-dimensional data. The fundamental principle underlying the present multidimensional associative learning is to regard multidimensional data as an ensemble of zero-dimensional data, wherein the associative learning process differentiates the initial zero-dimensional data into those to be learned, forgotten, or maintained. As an example, we use alphabet characters represented by a 5×5 binary matrix consisting of 25 bits. Each pixel in the matrix is assigned to a single memristor, giving a total of 25 memristors in the configuration, where black and white pixels are assigned to the HCS and LCS of G_{1-3} conductance states, respectively. As illustrated in Figure 4a, in the present experiment, a black-and-white 5×5 pattern representing the unconditioned stimulus character “R” is prepared as the initial state and is conditioned by the character “S” serving as the conditioned stimulus. The conditioning rule is applied uniformly to all memristors corresponding to each pixel: for both the unconditioned stimulus pattern (“R”) and the conditioned stimulus pattern (“S”), negative write voltages are applied to pixels designated as black (HCS) and positive voltages are applied to pixels designated as white (LCS). Pixel-wise state changes under this rule are classified into four types, which are summarized in Table 1. In the actual operation, unconditioned stimulus voltage V_4 corresponding to the “R” pattern is applied to T4, and conditioned stimulus voltage V_1 corresponding to the “S” pattern is applied to T1 of each memristor, thereby conditioning the initial “R” pattern to transform into “S”. The unconditioned stimulus (V_4) is co-applied once every ten conditioned stimulus (V_1) inputs. Voltage application protocols for the four types of state changes and the expected oxygen vacancy distribution are shown in Figure 4b.

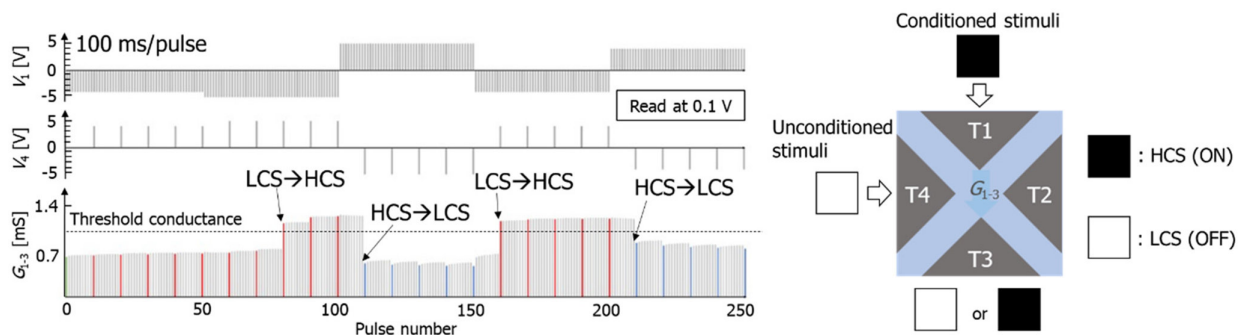


FIGURE 3 | Voltage pulse protocol emulating the bidirectional conditioning and the resulting conductance change of G_{1-3} under the voltage amplitude conditions of (V_1, V_4) = (−4, +4), (−5, +5), and (+5, −5 V).

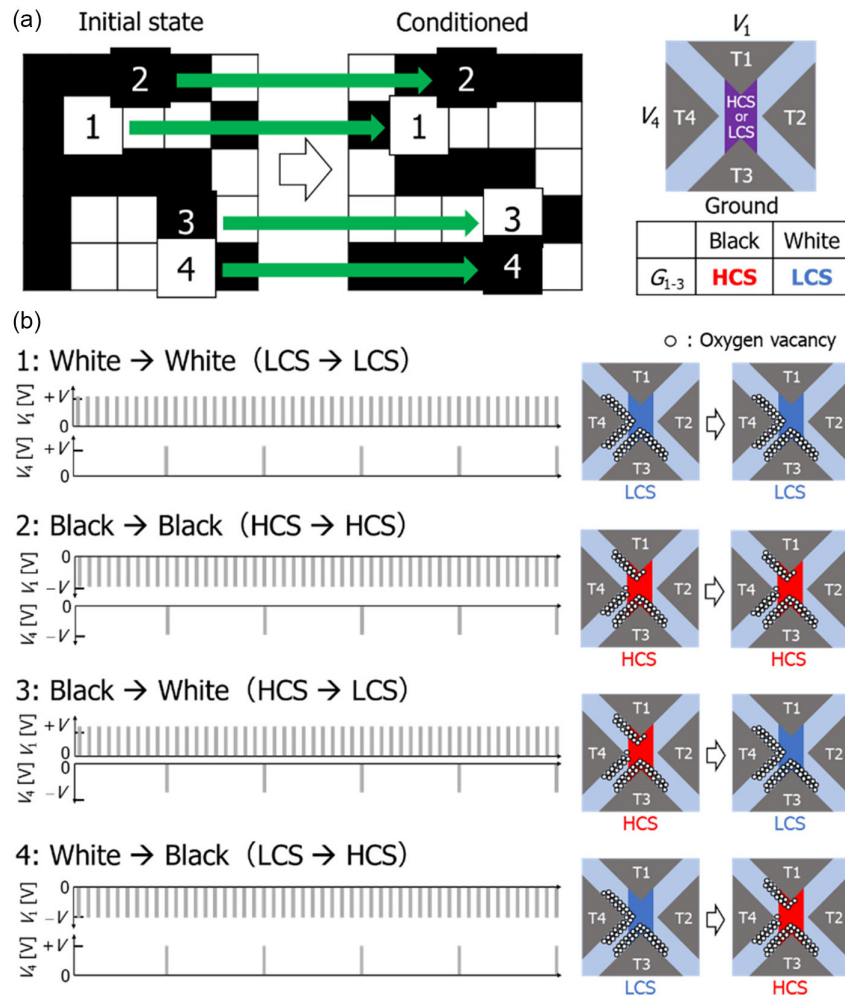


FIGURE 4 | (a) Multidimensional conditioning of 5×5 binary matrix data from the unconditioned stimulus character “R” (initial state) to the conditioned state character “S”. Black and white pixels are assigned to HCS and LCS of G_{1-3} conductance states, respectively. (b) Voltage application protocols for the four types of state changes and expected oxygen vacancy distribution during the operation.

TABLE 1 | Classification of pixel-wise state changes under the conditioning rule.

Type	Transition	Conductance state	Description
(i)	White → White	LCS → LCS	No change (remains in LCS)
(ii)	Black → Black	HCS → HCS	No change (remains in HCS)
(iii)	White → Black	LCS → HCS	Forward conditioning
(iv)	Black → White	HCS → LCS	Reverse conditioning

Figure 5 presents the results of associative learning from pattern “R” to “S,” achieved by simultaneously operating 25 memristors. Figure 5a shows the change in the G_{1-3} conductance map across the 25 memristors during the learning process, while Figure 5b,c display the corresponding individual conductance values and representative optical micrographs illustrating the electrocoloring of four selected memristors (labeled A, B, C, and D in Figure 5a) that exemplify the state transitions summarized in Table 1. Prior to preparing the initial pattern “R,” all 25 memristors were initialized to a target conductance of 0.6 mS (LCS), with an average and standard deviation of 0.62 and 0.037 mS, respectively, indicating good device homogeneity. In the initial state, each memristor represents either HCS (black pixel) or LCS (white pixel), with a threshold

conductance of 0.9 mS. These conductance states are verified by the electrocoloring patterns: in pixels A and C, oxygen vacancies accumulate near T3 and T4 and are depleted between T1 and T3, resulting in LCS, while in pixels B and D, vacancies accumulate near T1 and T3, yielding HCS (Figure 5b,c). During the conditioning process, associative inputs are applied to T1 and T4, and state transitions occur at each pixel according to the scheme shown in Figure 4. As shown in Figure 5a,b, the conversion from “R” to “S” is incomplete after the first and second conditioning cycles (pulse #10 and #20) but is nearly complete after the third conditioning (pulse #30). After the fourth and fifth conditioning, conditioned states are stably retained (results after the fifth conditioning are shown in Figure S2).

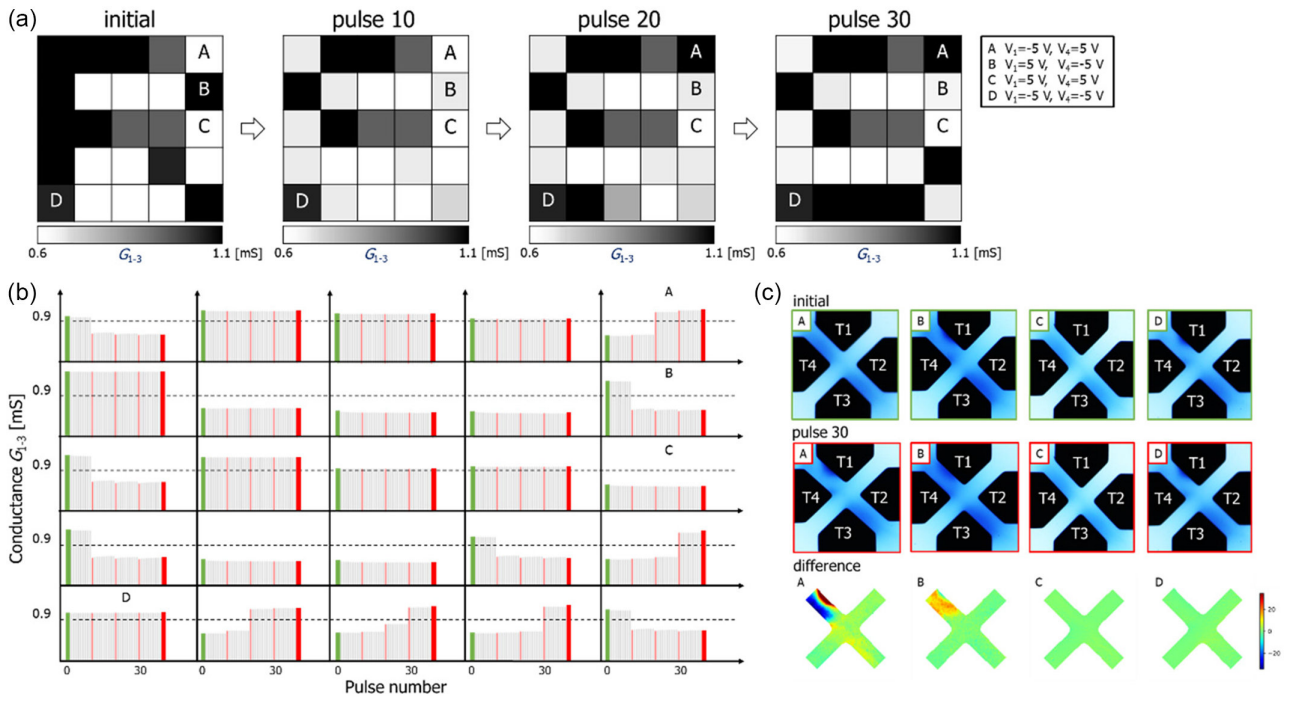


FIGURE 5 | Results of associative learning from 5×5 binary matrix patterns “R” to “S,” achieved by simultaneously operating 25 memristors. (a) Change in the G_{1-3} conductance map across the 25 memristors from initial state to the conditioned state at pulse 30. (b) Individual conductance values in 25 memristors. (c) Representative optical micrographs showing the electrocoloring of four selected four-terminal planar memristors. Difference maps are taken between the initial and pulse 30 states.

The electrocoloring observed in memristors A to D reflects changes in oxygen-vacancy distribution induced by conditioning: in pixel B, a partial drift of vacancies from T1 to T4 is observed after the first conditioning, as seen in the optical micrographs and difference maps (generated using anchor-point-based image registration [29]), which show decreased coloration near T1 and a corresponding decrease in G_{1-3} . Conversely, in pixel A, a partial drift of vacancies from T4 to T1 is observed after the third conditioning, with increased coloration near T1 and an increase in G_{1-3} (Figure 5c). In contrast, pixels C and D show little change in vacancy distribution throughout the conditioning process, which leads to negligible changes in G_{1-3} in such pixels. As shown in Figure 2b,c, conductance switching in this four-terminal memristor architecture occurs when the absolute value of the applied write voltage exceeds approximately 5V. Thus, the observed redistribution of oxygen vacancies can be attributed to a field-driven drift mechanism, where the vacancy configuration remains stable under equal potentials between T1 and T4 but shifts once the applied potential difference surpasses the threshold voltage. The present results of multi-dimensional conditioning with 25 memristors shown in Figure 5a,b also represent device-to-device variation among 25 devices. From Figure 5, we observe that the learning process is rather homogeneous; the forward conditioning (white to black) was attained in two or three learning processes (20 or 30 pulses), and the reverse conditioning (black to white) was attained after one conditioning process (10 pulses) in targeted devices. While we see some variation in resistance values in each device, necessary cycles for conditioning among different devices are consistent. So, the effect of device-to-device variation is moderate as far as we focus on binary (two-state) conditioning operation with multiple bits. Controllability of two-dimensional oxygen

vacancy distribution with a non-filamentary mechanism is the key to stable operation of multi-input associative functions in the present memristor system.

Finally, we discuss several aspects concerning integration and scaling of the four-terminal device. We emphasize that one important feature of the present four-terminal device is that its mechanism is clearly based on the 2D redistribution of oxygen vacancy (V_O^{2+}), and the resistance change is deterministic. This enables high-resolution analog memory operation. We have demonstrated that it can realize very high-resolution multi-level analog operation up to 512 resistance levels by combining feed-forward pulse voltage schemes [24]. Such performance cannot be readily attained by other kinds of devices than the present four-terminal memristor. By integrating the four-terminal devices, multidimensional associative learning is implementable without requiring external circuits (comparison with several previously reported associative learning memristor systems is shown in Table S1). On the other hand, the four-terminal structure may bring an increased device area and writing operation complexity. An increased footprint of the four-terminal memristors can be compensated by increased analog resistance resolution or more degrees of freedom in the internal dopant distribution topology. Also, further scaling the electrode spacing into the submicron regime by photolithography is expected to substantially reduce the switching time, possibly enabling sub-millisecond operation. In operation in an integrated cross-bar array, sneak path currents or cross-talk will be potential issues. Isolation of the individual four-terminal cells and stacking the selector layer with nonlinear characteristics onto the memristive layer are remedies for the problem. Further optimization of device geometry, operating voltage, and switching speed through device scaling will be the subject of future work.

4 | Conclusion

Using a four-terminal TiO_{2-x} memristor architecture, we demonstrated (i) stable non-filamentary resistive switching governed by two-dimensional oxygen-vacancy control, (ii) bidirectional Pavlovian conditioning including both learning and forgetting within a single device, and (iii) multidimensional associative learning of two-dimensional images through simultaneous operation of multiple devices. Importantly, all associative learning processes were realized solely by the proposed memristor architecture without any auxiliary computational or control circuitry. The memristor thereby functions not merely as a synapse emulator but as a self-contained learning and memory unit that autonomously acquires, stores, and updates associations between inputs. These findings outline a concrete pathway toward device-level implementation of higher-order associative functions and open prospects for scaling to higher dimensionality, multilevel weights, and adaptive network operation in fully hardware-based learning systems.

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Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Supporting Information

Additional supporting information can be found online in the Supporting Information section.